In the Claims

Claims 1-11 **(Canceled)**

Claim 12 **(Currently Amended)** A semiconductor arrangement comprising a bump electrode having a first protrusion and a second protrusion bonded to an IC electrode on a circuit forming surface of a semiconductor element,

wherein said first and second protrusions are in contact with or close to an electrode on a circuit board when the semiconductor element is mounted on the circuit board,

wherein said first protrusion has a formed portion formed by forming a melted portion of a wire with a capillary and solidifying the melted portion, and a wire material portion comprising a portion of the wire in a vicinity of the melted portion, said wire material portion extending from a vertex portion of said formed portion downward from said vertex portion and being bonded to said formed portion, ~~and~~

wherein said wire material portion does not contact the IC electrode or the circuit forming surface, and

wherein said bump electrode is approximately V-shaped, and a bottom portion of the 'V' faces towards the semiconductor element.

Claim 13 **(Previously Presented)** A semiconductor arrangement as claimed in claim 12, wherein the electrode on the circuit board and said bump electrode are electrically connected to each other.

Claims14-20 **(Canceled)**

Claim 21 **(Previously Presented)** A semiconductor arrangement as claimed in claim 12, wherein said first and second protrusions have an amount of conductive adhesive by which the IC electrode of the semiconductor element can be connected to said bump electrode.

Claim 22 **(Previously Presented)** A semiconductor arrangement as claimed in claim 12, wherein said vertex portion of said first protrusion has a flat surface portion and a vertex portion of said second protrusion has a flat surface portion.

Claim 23 **(Previously Presented)** A semiconductor arrangement as claimed in claim 22, wherein said flat surface portion of said first protrusion and said flat surface portion of said second protrusion have substantially a same height.

Claim 24 **(Previously Presented)** A semiconductor arrangement as claimed in claim 12, wherein said second protrusion is formed from a portion of the wire extending upward from said wire material portion bonded to said formed portion.

Claim 25 **(New)** A semiconductor arrangement comprising a bump electrode having a first protrusion and a second protrusion bonded to an IC electrode on a circuit forming surface of a semiconductor element,

wherein said first and second protrusions have substantially a same height and are either both in contact with or substantially equally close to an electrode on a circuit board when the semiconductor element is mounted on the circuit board,

wherein said first protrusion has a formed portion formed by forming a melted portion of a wire with a capillary and solidifying the melted portion, and a wire material portion comprising a portion of the wire in a vicinity of the melted portion, said wire material portion extending from a vertex portion of said formed portion downward from said vertex portion and being bonded to said formed portion, and

wherein said wire material portion does not contact the IC electrode or the circuit forming surface.

Claim 26 **(New)** A semiconductor arrangement as claimed in claim 25, wherein the electrode on the circuit board and said bump electrode are electrically connected to each other.

Claim 27 **(New)** A semiconductor arrangement as claimed in claim 25, wherein said first and second protrusions have an amount of conductive adhesive by which the IC electrode of the semiconductor element can be connected to said bump electrode.

Claim 28 **(New)** A semiconductor arrangement as claimed in claim 25, wherein said vertex portion of said first protrusion has a flat surface portion and a vertex portion of said second protrusion has a flat surface portion.

Claim 29 **(New)** A semiconductor arrangement as claimed in claim 25, wherein said second protrusion is formed from a portion of the wire extending upward from said wire material portion bonded to said formed portion.

Claim 30 **(New)** A semiconductor arrangement comprising a bump electrode having a first protrusion and a second protrusion bonded to an IC electrode on a circuit forming surface of a semiconductor element,

wherein said first and second protrusions are in contact with or close to an electrode on a circuit board when the semiconductor element is mounted on the circuit board,

wherein said first protrusion has a formed portion formed by forming a melted portion of a wire with a capillary and solidifying the melted portion, and a wire material portion comprising a portion of the wire in a vicinity of the melted portion, said wire material portion extending from a vertex portion of said formed portion downward from said vertex portion and being bonded to said formed portion,

wherein said wire material portion does not contact the IC electrode or the circuit forming surface, and

wherein said vertex portion of said first protrusion has a flat surface portion parallel to the IC electrode and a vertex portion of said second protrusion has a flat surface portion parallel to the IC electrode.

Claim 31 **(New)** A semiconductor arrangement as claimed in claim 30, wherein the electrode on the circuit board and said bump electrode are electrically connected to each other.

Claim 32 **(New)** A semiconductor arrangement as claimed in claim 30, wherein said first and second protrusions have an amount of conductive adhesive by which the IC electrode of the semiconductor element can be connected to said bump electrode.

Claim 33 **(New)** A semiconductor arrangement as claimed in claim 30, wherein said flat surface portion of said first protrusion and said flat surface portion of said second protrusion have substantially a same height.

Claim 34 **(New)** A semiconductor arrangement as claimed in claim 30, wherein said second protrusion is formed from a portion of the wire extending upward from said wire material portion bonded to said formed portion.

Claim 35 **(New)** A semiconductor arrangement as claimed in claim 12, wherein said first protrusion comprises a first top portion of the 'V', said second protrusion comprises a second top portion of the 'V', and said first and second protrusions are adapted to be directly electrically connected to the circuit forming surface of the semiconductor element.